SUBJECT: Memory Requirements for the Launch Vehicle Digital Computer (LVDC) - Case 330

DATE: April 25, 1967

FROM: J. J. Rocchio

ABSTRACT

The Launch Vehicle Digital Computer (LVDC) has a modular memory system with a maximum capacity of eight modules. Each module has 16 sectors, for a total of 28 sectors (64 duplexed sectors) in all.

Memory requirements have grown to the point that, although four modules were flown on AS 201, eight are planned for AS 501-504. The possibility of depletion of all memory reserves has led to:

1. studies of memory augmentation methods;
2. reevaluation of current and anticipated memory requirements;
3. consideration of some reprogramming to utilize memory more efficiently.

At this time, expected reserve capacity in the LVDC memory is about 18% (12.9 sectors duplex) of total capacity for AS 501, and only 11% (6.9 sectors duplex) for AS 504. This is considered insufficient to provide an adequate margin for new requirements and contingencies. It is therefore recommended that the memory savings identified in the IBM LVDC Memory Utilization Study as being "readily obtainable" be implemented. This action would increase the reserve to 31% (19.6 sectors duplex) for AS 501 and 24% (15.2 sectors duplex) for AS 504. Additional study of future Saturn operations is needed to establish requirements for a Saturn V Auxiliary Memory Unit.

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MEMORANDUM FOR FILE

BACKGROUND

The Saturn Launch Vehicle Digital Computer (LVDC) utilizes a coincident current core memory with a 28 bit word length (including two parity bits). Each memory word can store two 13 bit instructions or a 26 bit data word. The memory system is modular, each module containing 4096 words with a maximum capacity of eight modules.

The memory system is designed to allow duplex operation (concurrent readout from a pair of modules with the capability of correcting single errors) as well as conventional simplex operation. Duplex operation of the memory complements the triply modular redundant (TMR) logic of the LVDC and is incorporated for increased reliability. In the duplex mode, the maximum capacity of the memory system is 16 K words (capable of storing 32 K instructions). The machine design allows for independent duplex/simplex instruction access and data access under program control. Current programming practice requires all flight programs to be operated in the duplex mode; most preflight routines, however, are operated in the simplex mode. The memory area used for preflight routines is used in flight for temporary storage of telemetry data.

MEMORY REQUIREMENTS/USAGE

During the original program definition stages, estimates* of the memory requirements for the LVDC indicated that four modules (2 duplex) would be sufficient for Apollo. This estimate envisioned 1 - 1.5 modules (duplex) for flight programs with the remaining used for preflight. Actual usage (in number of modules flown) to date has been:

AS 201 - 4 modules

AS 203 - 4 modules

AS 202 - 6 modules

*As cited in the Final Report, Saturn V LVDC Auxiliary Memory Study (NASA Contract NAS-8-11562), IBM Federal Systems Division, October 28, 1966.

[redacted]

and current planning calls for:

AS 206 - 6 modules

AS 501-504 - 8 modules

The increasing trend in LVDC memory usage was such that Marshall Space Flight Center (MSFC) awarded a study contract to IBM to consider means of providing auxiliary memory for the LVDC. This study was carried out during June - September, 1966, and a final report was issued in October 1966. The study ground rules allowed no LVDC/LVDA modifications and required that at least 32 K (100% increase) of additional memory be furnished. Three alternative auxiliary memory systems were considered by IBM: core, tape, and drum. The drum system was recommended.

A part of this IBM study considered the memory requirements for the LVDC. It was concluded that eight modules would just support the AS 200 series of flights, but would be inadequate for the AS 500 series. The largest single factor contributing to the increased memory requirements as considered by IBM was the set of routines designated as the Hardware Evaluation Program (HEP). These programs operate in orbit when the vehicle is not over a ground station and encompass a set of independent test programs designed to evaluate the performance of flight hardware. The requirements part of the IBM study allocated 24.25 sectors to these routines (each LVDC memory module contains 16 sectors of 256 words). Based on a thorough evaluation by MSFC, requirements for the HEP routines have been relaxed. Current projections for AS 501-504 allocate less than two sectors for HEP routines.

MAS PARTICIPATION

In January 1967, MAS, at the request of Mr. F. S. Wojtalik of Astrionics-NASA-MSFC, agreed to provide assistance in determining the present and anticipated memory requirements for the LVDC. To this end, beginning in February 1967, several working meetings were arranged, attended by representatives from IBM, MSFC/R-ASTR-N, and MAS. In the course of these meetings the actual and projected memory usage for AS 206 and AS 501-504 were reviewed in detail. In addition, a number of potential means for reducing memory usage were proposed by IBM, MSFC/R-ASTR-N, and MAS. Specifically, these could be categorized under the headings of:

1. deletion of programs,

2. simplification of programs,

3. more efficient program organization,

4. simplex instead of duplex operation,

5. segmentation and overlay of preflight programs.

IBM/Huntsville has provided* a detailed analysis of the potential memory savings and associated cost and implications of applying these techniques to a number of specific candidate programs. This information provides the ability to immediately gain additional reserve memory capacity (at the cost of some reprogramming effort), and to evaluate a number of potential memory savings against overall LVDC requirements.

PHASE II - IBM STUDY

In March 1967, IBM undertook an extension of the study of design concepts for a Saturn LVDC Auxiliary Memory Unit. This Phase II effort is considering AMU designs under the following constraints:

1. Modification of the LVDC is allowed.

2. At least 100 K words of additional storage are to be provided.

3. Concurrent load/compute operation is required.

4. Primary consideration is to be directed to a tape/core-buffer configuration.

It is significant to note that a tape/core-buffer AMU system is also being considered for the Apollo Guidance Computer and that this Phase II study effort requires IBM to evaluate the Apollo tape unit for the LVDC AMU application.

SUMMARY AND CONCLUSIONS

At the present time, it appears that the memory requirements (known and anticipated) for the Apollo Program (through AS 504) can be supported by the current configuration (LVDC with eight memory modules). (This conclusion differs from that reached by IBM in the Phase I LVDC AMU study due to the significant change in the HEP requirements.)

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*LVDC Memory Utilization Study (rough draft) IBM/Huntsville, April 1967.

However, projections* for AS 504 based on the current program configuration indicate a reserve of only 6.9 sectors (duplex) or about 11% of the total LVDC memory capacity of 64 sectors (duplex). As new requirements are primarily anticipated in the flight programs category, this reserve corresponds to a growth factor in terms of the flight programs allocation of about 14%. Spare capacity in this range is considered too low to provide a reasonable margin to satisfy new requirements and meet program contingencies. Therefore, based on the results of the memory conservation study, it is recommended that:

1. those memory saving programming changes which are relatively easy to incorporate and which have no appreciable impact on performance or operations be implemented;

2. the remaining memory conservation tasks be categorized with respect to feasibility and then ranked with respect to desirability based on amount of savings, cost, impact on facilities and operation, etc.;

3. a plan be established for implementing the required reprogramming to realize the savings from the feasible tasks identified in 2.

With the "relatively easy" program changes incorporated, projections* for AS 501 show a reserve capacity of 19.6 sectors or about 31% of the total LVDC capacity. For AS 504 the corresponding potential reserve is 15.2 sectors or about 24% of capacity. These figures correspond to growth factors in terms of flight program requirements of 56% for AS 501, and 38% for AS 504. Spare capacity in this range is considered to be sufficient to the degree that a high priority development program for the LVDC AMU is not required to support the Apollo program.

In considering LVDC memory requirements it should be noted that there are two conflicting trends at work. On the one hand, as flights proceed from the developmental to the operational phase, R & D-oriented requirements can be expected to disappear or diminish. On the other hand, as the system matures there will be a tendency to resist hardware changes, thus placing the burden of meeting new requirements on the software. Planned reserves, together with the readily obtainable savings indicated by the memory conservation study

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*Projected memory allocations for the LVDC are derived in the Appendix.

and the ability to achieve even further savings, should be adequate to meet such contingencies for the near term, assuming effective controls are maintained on the imposition of new requirements on the LVDC.

Future Saturn operations then, are likely to be critical in determining the need and timing required for a production phase AMU program. To this end it is recommended that LVDC requirements for support of the AAP Program be studied at the earliest opportunity.

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1031-JJR-sjh

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Attachment
Appendix

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APPENDIX

LVDC Memory Allocation Projections for AS 501-504

A. Current Status AS 501*

Routine	Sectors Allocated	Reserve Distributed Core Locations (included in sector allocation)
Prelaunch	9	
Boost	11	286
Orbit (Flight)	5	111
Orbit (Orbital)	9.5	153
Common	16.5	196
	51.0	746

Projected Requirements AS 501*

Current 501	51	746
Switch Selector	1.5	
Orbital Guidance	1.5	
	54.0	746

B. Projected Requirements AS 504

Projected 501	54	746
Variable Launch Azimuth	2	
Alternate Restart Time Bases	2	
Guidance Update	1	
Guidance Switchover	1	
	60	746

C. Estimated Memory Savings

(Taken from IBM rough draft of LVDC Memory Utilization Study, April 1967)

C.1 Obtainable with small or moderate cost and negligible or slight impact on operations or performance.

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*Taken from IBM working papers, February 1967.

Appendix (Cont'd)

Routine	Core Locations Saved AS 501	Core Locations Saved AS 504
Switch Selector	380	572
Telemetry Executive	100	300
Revised Data Compression	115	115
Simplex Boost Initialization, Simulated Flight, and Variable Targeting	360	360
Use of Subroutines in Minor Loop	200	200
Simplified Atmospheric Drag Model	65	65
Use of Subroutines in Navigation Routine	150	150
Deletion of LVDC Self-Test	352	352

C.2 Obtainable with large implementation cost and moderate impact on launch operations.

Overlay Part of Flight Program with Early Prelaunch Routines	768	768

Total Savings (locations)	AS 501	AS 504
Category C.1	1722	2114
Categories C.1 and C.2	2490	2882

Table A.1 summarizes the projected allocations for AS 501 and 504 showing the effects of both Category C.1 and Category C.2 savings.

	Total Allocated		Spare		Flight Programs		Spare	Spare
	Locations	Sectors	Locations	Sectors	Locations	Sectors	Total	Flight
Projected 501	13,078	51.1	3,306	12.9	10,774	42.1	18%	31%
Projected 501 with Category C.1 Savings	11,356	44.4	5,028	19.6	9,052	35.4	31%	56%
Projected 501 with Categories C.1 and C.2 Savings	10,588	41.4	5,796	22.6	9,052	35.4	35%	64%
Projected 504	14,614	57.1	1,770	6.9	12,310	48.1	11%	14%
Projected 504 with Category C.1 Savings	12,500	48.8	3,884	15.2	10,196	39.8	24%	38%
Projected 504 with Categories C.1 and C.2 Savings	11,732	45.8	4,652	18.2	10,196	39.8	28%	46%

TABLE A1 - PROJECTED LVDC CORE ALLOCATIONS